Claims 48-72 were rejected under 35 U.S.C. 103 as unpatentable over U.S. Patent No. 6,001,538 to Chen et al. taken with U.S. Patent No. 5,960,306 to Hall et al. Claims 50-51 have been canceled without prejudice. Claims 48-49, 52-56, 58, 61-68, 70 and 72 have been amended for clarity and to emphasize certain features of embodiments of the invention. Applicant respectfully submits that the Examiner cited no portion of the art suggesting the combination of elements including at least the etchant and the shape of the opening as recited in the claims, as amended. For at least the above reasons, applicant respectfully requests that the rejection be withdrawn.

New dependent claims 73-74 have been added. Support for these claims may be found throughout the specification and figures. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the amendments to the claims made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 48-49 and 52-74 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes — **Jan. 31, 2003** **Date**

Version With Markings to Show Changes Made

Claims 48-49, 52-56, 58, 61-68, 70 and 72 were amended as follows:

48. (amended) A method of fabricating a semiconductor device comprising:

forming a pad;

forming a protective insulating region on the pad [by forming] including first and second insulating layers, the first insulating layer being in direct contact with the pad and the second insulating layer being in direct contact with the first insulation layer; the second insulating layer comprising silicon nitride;

forming a mask layer on the protective insulating region in direct contact with a surface of the second [insulation] insulating layer, the second [insulation] insulating layer being positioned between the first insulating layer and the mask layer, the mask layer including an aperture in a region corresponding to an electric connection region of the pad; and

dry etching through the surface of the second [insulation] insulating layer at the aperture in the mask to form an opening extending through the second insulating layer and the first insulating layer to the pad, wherein an etchant gas comprising CF_4 and O_2 is used to form the opening extending through the second insulation layer, and wherein at least a portion of the opening has a tapered shape.

49. (amended) A method as in claim 48, wherein the dry etching comprises [a first isotropic etching operation and a second anisotropic etching operation] isotropically etching at least a portion of the second insulating layer and anisotropically etching at least a portion of the first insulating layer.

52. (amended) A method as in claim 48, wherein at least a side surface of the second [protective] insulating layer surrounding the electric connection region has a tapered surface with an acute angle to the top surface of the pad after the dry etching.

53. (amended) A method as in claim [53] 48, wherein an angle [between] of the side surface of the second [protective] insulating layer surrounding the opening [electric connection region and the top surface of the pad] is smaller than a tapered angle [between] of a side surface of the first [protective] insulating layer surrounding the [electric connection region and the top surface of the pad] opening.

54. (amended) A method as in claim 48, wherein an angle between a side surface of the second [protective] insulating layer surrounding [the electric connection region] opening and a top surface of the pad is in the range of 30° to 60°..

55. (amended) A method as in claim 54, wherein an angle between a side surface of a portion of the first [protective] insulation layer surrounding the [electric connection region] opening and the top surface of the pad is in the range of 60° to 90°.

56. (amended) A method as in claim 48, wherein a distance between an upper end of a side surface of the first [protective] insulating layer surrounding the [electric connection region] opening and a lower end of the side surface of the second [protective] insulating layer surrounding the opening [electric connection region] is in the range of 0 μm to 3 μm.

58. (amended) A method as in claim 48, wherein an aperture formed in the second [protective] insulating layer after the dry etching is larger than an aperture formed in the first [protective] insulating layer after the dry etching.

61. (amended) A method as in claim 60, wherein the same etchant gas is used to etch the first insulating layer and the second insulating layer. [48, comprising forming the second insulating layer from a material comprising silicon nitride].

62. (amended) A method as in claim 61, wherein the first insulating layer and the second insulating layer are etched in a continuous manner. [48, comprising forming the second

protective insulating layer from a material comprising a nitride oxide layer].

63. (amended) A method as in claim 48, wherein the first insulating layer and the second insulating layer are etched in a continuous manner. [48, comprising forming the pad on an insulation layer].

64. (amended) A method for forming a bonding pad area using a dry etch process, comprising:

forming a conducting pad in electrical contact with an electronic device;

forming a protective insulation layer on a surface of the conducting pad, the protective insulation layer including at least first and second insulating layers, wherein the first insulating layer and the second insulating layer are formed from materials having different compositions, the first insulating layer comprising a silicon oxide layer, the second insulating layer comprising a silicon nitride layer, the silicon oxide [first insulating] layer being formed [in direct contact with] on [the surface of] the conducting pad, the silicon nitride [second insulating] layer being formed [in direct contact with] on the silicon oxide [first insulating] layer;

forming a mask in direct contact with a surface of the protective insulation layer and providing an opening in the mask; and

dry etching through the surface of the protective insulation layer at the opening in the mask to form an aperture extending through the [second insulating] silicon nitride layer and the [first insulating] silicon oxide layer to the surface of the pad using CF_4 and O_2 as an etchant, so that the [second insulating] silicon nitride layer includes a side surface surrounding the aperture, the [second insulating] silicon nitride layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to the surface of the conducting pad, and the [first insulating] silicon oxide layer includes a side surface surrounding the aperture, the [first insulating] silicon oxide layer side surface having a tapered shape with an angle in the range of 60 degrees to 90 degrees in relation to the surface of the conducting pad.

65. (amended) A method as in claim 64, wherein the protective insulation layer consists of the first insulating layer and the second insulating layer, the first insulating layer consisting of a silicon oxide layer and the second insulating layer consisting of a silicon nitride

layer.

66. (amended) A method as in claim 65, wherein the dry etching includes continuously etching the second insulating layer and the first insulating layer [first insulating layer comprises an oxide and the second insulating layer comprises a nitride].

67. (amended) A method as in claim 64, wherein the dry etching includes [an] isotropic etching of at least part of the silicon nitride layer [operation followed by] and [an] anisotropic etching of at least part of the silicon oxide layer [operation].

68. (amended) A method of fabricating a semiconductor device comprising:

forming a pad with a predetermined pattern on an insulating layer;

forming a protective insulating layer on a surface of the pad;

forming a mask layer in direct contact with a surface of the protective insulating layer, the mask layer having an aperture in a region corresponding to an electrical connection region of the pad; and

dry etching through the [surface of the] protective insulating layer using an etchant comprising CF_4 and O_2 to form an opening extending through the protective insulating layer to the electrical connection region of the pad, so that the protective insulating layer includes a side surface surrounding the opening, the side surface being tapered so that [a diameter] the opening of the protective insulation layer at the pad surface is smaller than [a diameter] the opening of the protective insulation layer a distance away from the pad surface.

70. (amended) The method of fabricating a semiconductor device of claim 68, wherein a tapered angle between the side surface of the insulating layer surrounding the [electric connection region opening and the top surface of the pad] opening is in the range of 10° to 80°.

72. (amended) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from [a material including] one of a silicon oxide layer and a silicon nitride layer.